Listing of the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-17. (Cancelled)

18. (Previously presented) A fault-tolerant system on an integrated circuit, comprising:

a configurable logic array;

a boot program stored in a programmable memory region, which is executed during system initialization;

a mini-boot code stored in a protected memory region, which is an alternative set of system initialization instructions and executed when there is an error during an in-circuit program process, wherein the mini-boot code comprises a configuration load program designed to access a configuration data from a default location; and

a processor coupled to the programmable memory region, the protected memory region and the configurable logic array, for executing instructions from the programmable memory region or the protected memory region.

19. (Previously presented) The fault-tolerant system of claim 18, wherein the processor boots from the mini-boot code instead of the boot program if the system is rebooted during the in-circuit program process.

20. (Previously presented) The fault-tolerant system of claim 18, wherein the configurable logic array has a programmable configuration defined by configuration data stored in programmable configuration points within the configurable logic array.

21. (Previously presented) The fault-tolerant system of claim 18, wherein the processor takes a boot vector which points to the mini-boot code during system initialization when the in-circuit program process is not completed.

22. (Previously presented) The fault-tolerant system of claim 18, wherein the processor further couples to a remote host address register, which contains a backup copy of a remote host address.

23. (Previously presented) The fault-tolerant system of claim 18, further comprising a multiplexer coupled to the processor to select the boot program or the mini-boot code during system initialization according to an in-circuit program process status.

24. (Previously presented) The fault-tolerant system of claim 22, wherein the mini-boot code causes the processor to restart a configuration load process by reading the remote host address register to determine which remote host to contact in order to reinitiate the configuration load process.

25. (Previously presented) The fault-tolerant system of claim 18, wherein the default location is one of an on-chip non-volatile memory and a host expected to be coupled with the integrated circuit.

26. (Previously presented) A method for configuring a fault-tolerant system on an integrated circuit, the integrated circuit comprising a processor coupled to a programmable memory region, a protected memory region and a configurable logic array, the method comprising:

executing a boot program in a programmable memory region;

performing an in-circuit program process by executing a configuration handler to program the configurable logic array;

executing a mini-boot code in a protected memory region when there is an error during an in-circuit program process: and

providing a configuration load program designed to access a configuration data from a default location in the mini-boot code.

27. (Previously presented) The method of claim 26, wherein the processor boots from the mini-boot code instead of the boot program if the fault-tolerant system is rebooted during the in-circuit program process.

28. (Previously presented) The method of claim 26, wherein the processor takes a boot vector which points to the mini-boot code during system initialization when the in-circuit program process is not completed.

29. (Previously presented) The method of claim 26, wherein the mini-boot code causes the processor to restart a configuration load process by reading a remote host address register to determine which remote host to contact in order to reinitiate the configuration load process.

30. (Previously presented) The method of claim 26, wherein the default location is one of an on-chip non-volatile memory and a host expected to be coupled with the integrated circuit.